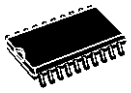
8. IC Block Digrams

8-1 Main

1. 74CX244

LOW VOLTAGE CMOS OCTAL BUS BUFFER (3-STATE) WITH 5V TOLERANT INPUTS AND OUTPUTS

- 5V TOLERANT INPUTS AND OUTPUTS
- HIGH SPEED:
  t_{PD} = 6.5 ns (MAX.) at V_{CC} = 3V
- POWER-DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 24 mA (MIN)
- PCI BUS LEVELS GUARANTEED AT 24mA
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2.0V to 3.6V (1.5V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 244
- LATCH-UP PERFORMANCE EXCEEDS 500mA
- ESD PERFORMANCE:
  HBM >2000V; MM > 200V



M
(Micro Package)

T
(TSSOP Package)

ORDER CODES :
74LCX244M 74LCX244T

DESCRIPTION

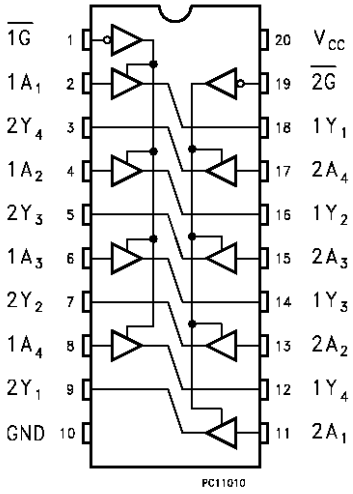
The LCX244 is a low voltage CMOS OCTAL BUS BUFFER (NON-INVERTED) fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology. It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for both inputs and outputs.

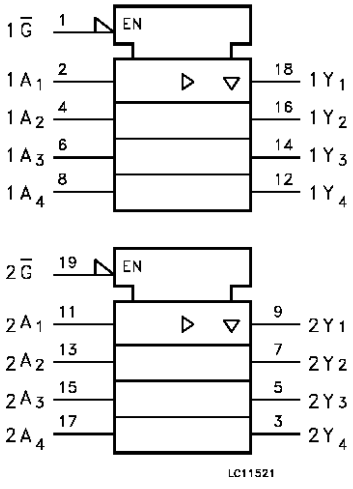
It has same speed performance at 3.3V than 5V AC/ACT family, combined with a lower power consumption.

This device is designed to be used with 3 state memory address drivers, etc.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS





74VHC244
Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The VHC244 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHC244 is a non-inverting 3-STATE buffer having two active-LOW output enables. These devices are designed to be used as 3-STATE memory address drivers, clock drivers, and bus oriented transmitter/receivers.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

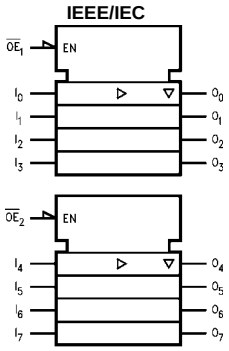
- High Speed: t_{PD} = 3.9ns (typ) at V_{CC} = 5V
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Power down protection is provided on all inputs
- Low noise: V_{OLP} = 0.6V (typ)
- Low power dissipation: I_{CC} = 4 µA (max) @ T_A = 25°C
- Pin and function compatible with 74HC244

Ordering Code:

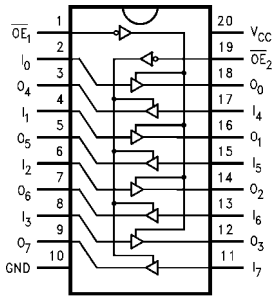
Order Number	Package Number	Package Description
74VHC244M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300î Wide
74VHC244SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC244MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC244N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300î Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter ìXî to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	3-STATE Output Enable Inputs
I_0ñI_7	Inputs
O_0ñO_7	3-STATE Outputs

74VHCT244A
Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The VHCT244A is an advanced high speed CMOS octal bus transceiver fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHCT244A is a non-inverting 3-STATE buffer having two active-LOW output enables. This device is designed to be used as 3-STATE memory address drivers, clock drivers, and bus oriented transmitter/receivers.

Protection circuits ensure that 0V to 7V can be applied to the input and output (Note 1) pins without regard to the supply voltage. These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up.

Note 1: Outputs in OFF-State

Features

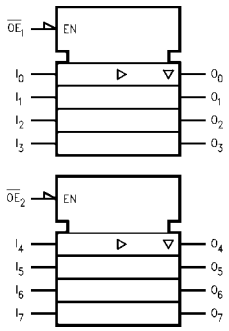
- High Speed: t_{PD} = 5.9 ns (typ) at V_{CC} = 5V
- Power down protection is provided on inputs and outputs
- Low power dissipation: I_{CC} = 4 µA (max) @ T_A = 25°C
- Pin and function compatible with 74HCT244

Ordering Code:

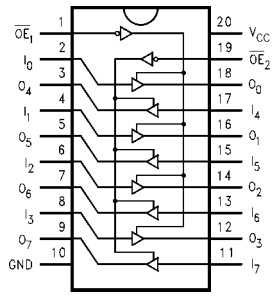
Order Number	Package Number	Package Description
74VHCT244AM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74VHCT244ASJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHCT244AMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHCT244AN	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter ìXî to the ordering code.

Logic Symbol



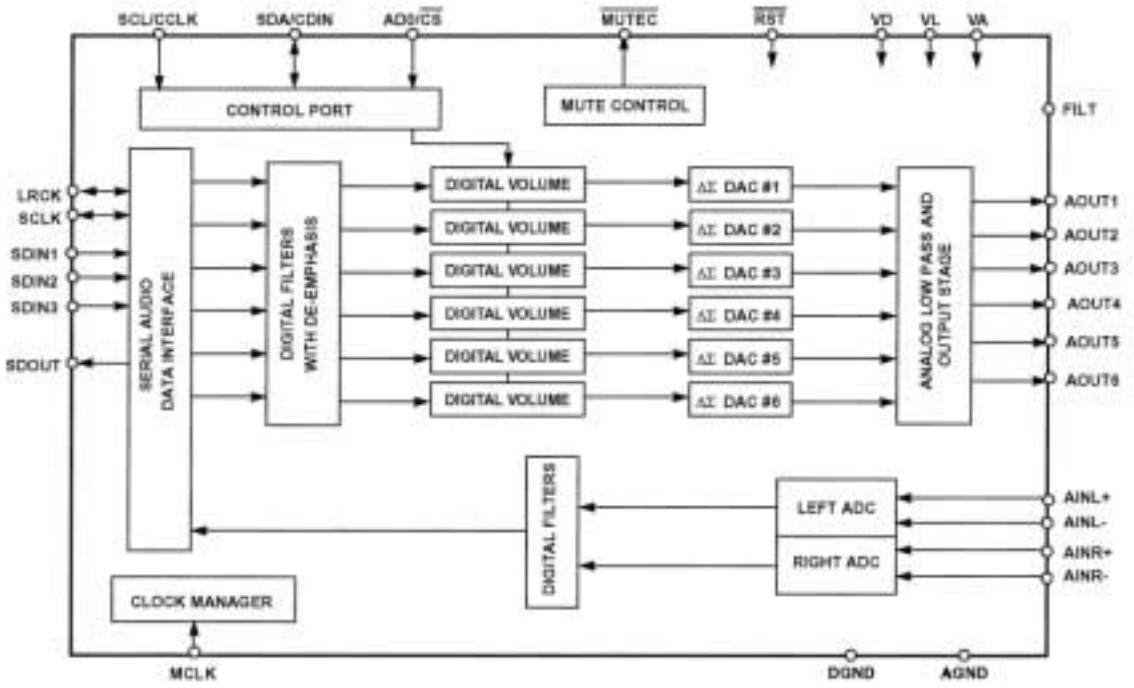
Connection Diagram



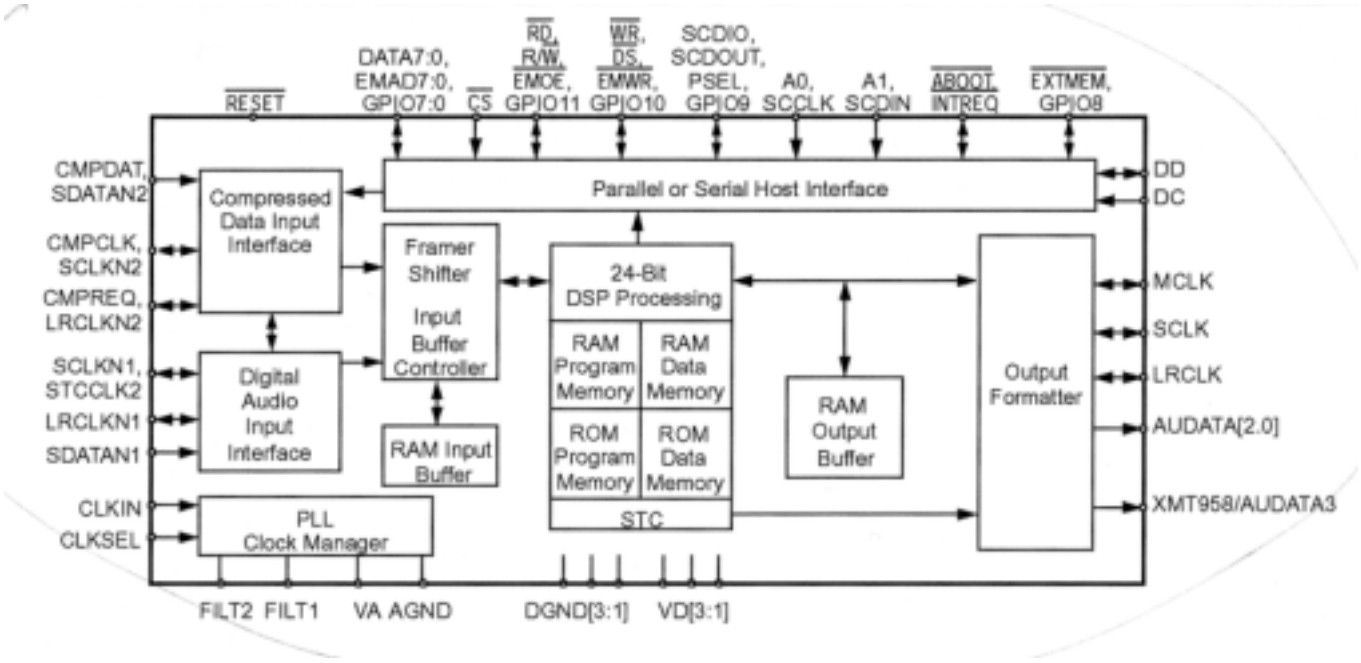
Pin Descriptions

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	3-STATE Output Enable Inputs
I_0ñI_7	Inputs
O_0ñO_7	3-STATE Outputs

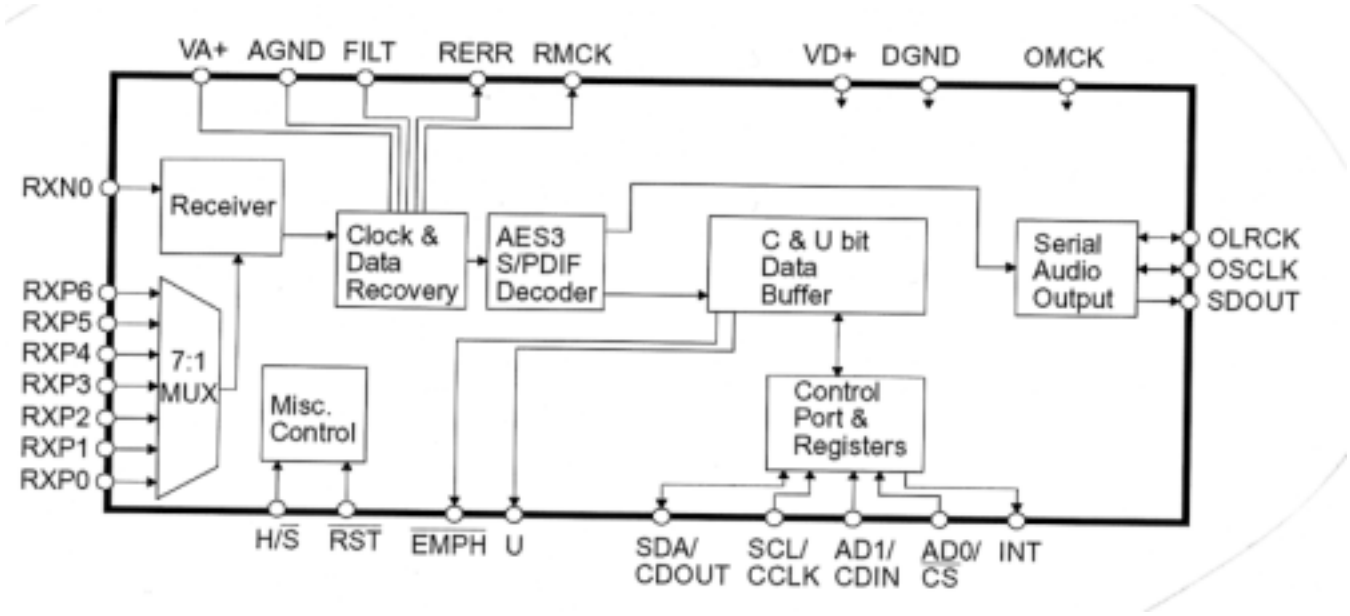
4. CS4228

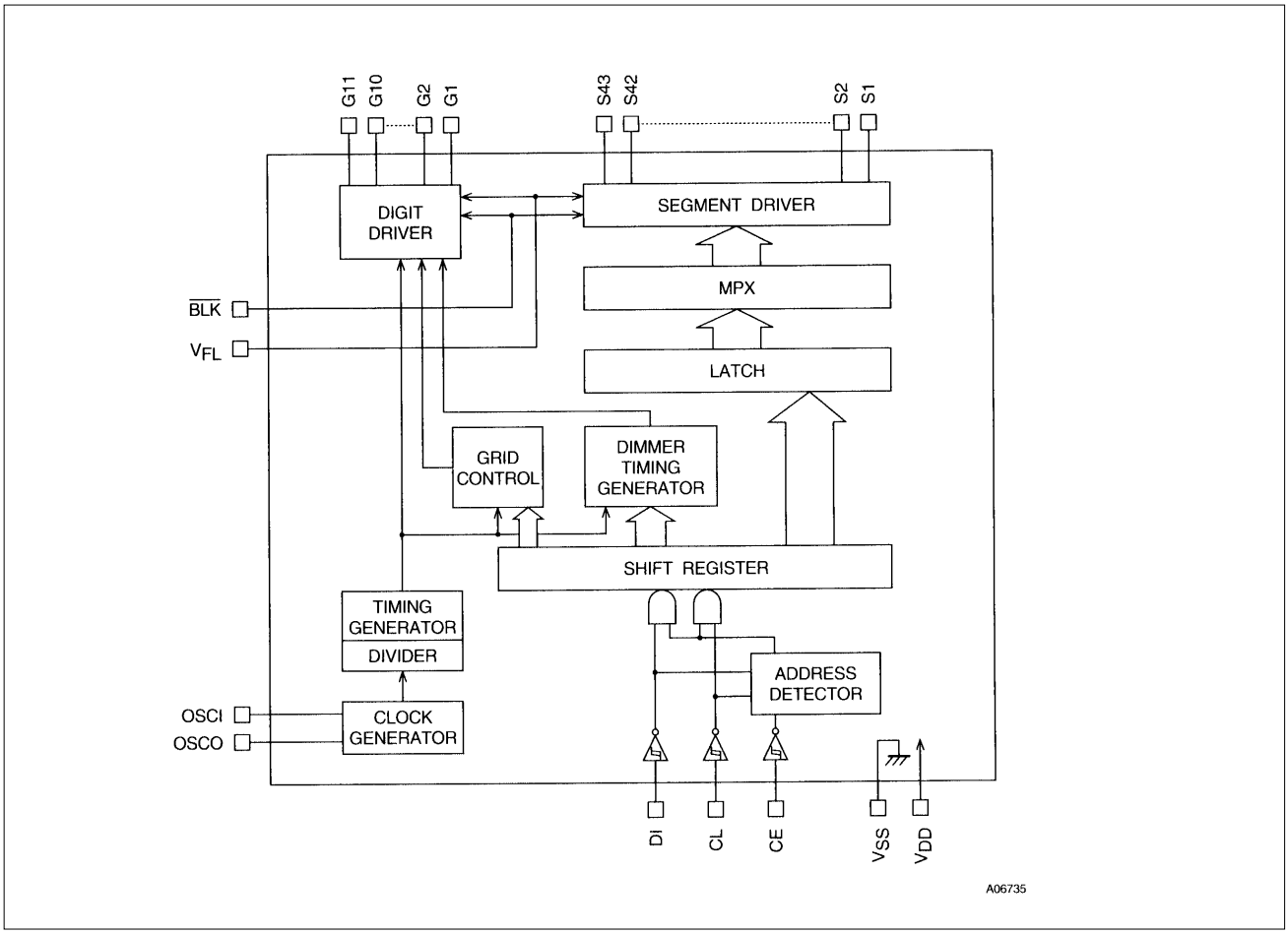


5. CS49300



6. CS8415A


VA+
AGND
FILT
RERR
RMCK
VD+
DGND
OMCK
RXN0
Receiver
Clock & Data Recovery
AES3 S/PDIF Decoder
C & U bit Data Buffer
Serial Audio Output
OLRCK
OSCLK
SDOUT
RXP6
RXP5
RXP4
RXP3
RXP2
RXP1
RXP0
7:1 MUX
Misc. Control
Control Port & Registers
H/S
RST
EMPH
U
SDA/ CDOUT
SCL/ CCLK
AD1/ CDIN
AD0/ CS
INT



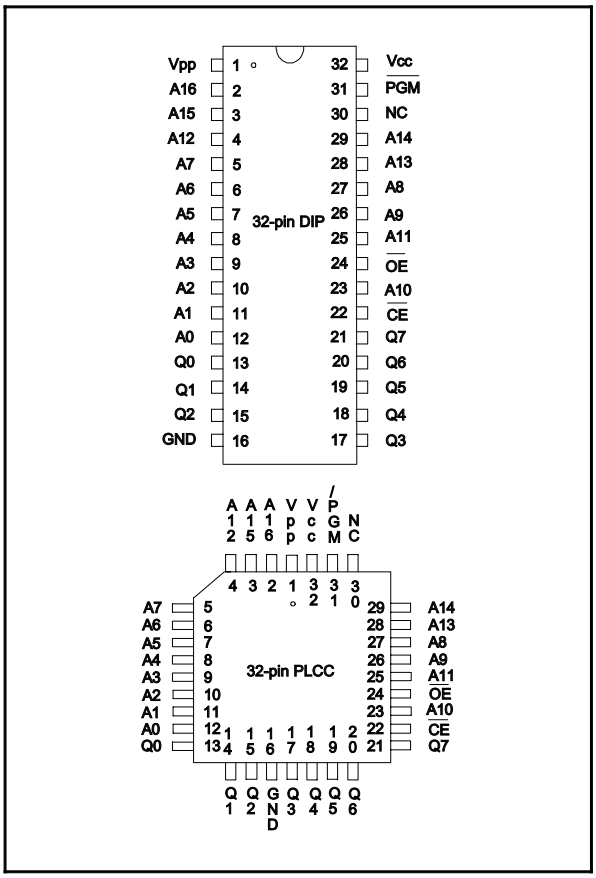
Pin Functions

Pin	Pin No.	Function	I/O	Handling when unused
V_{FL}	1, 13	Driver block power supply connection. (Both pins must be connected.)	—	—
V_{DD}	60	Logic block power supply connection. Provide a voltage between 4.5 and 5.5 V.	—	—
V_{SS}	57	Power supply connection. Connect to the ground.	—	—
OSCI	59	Oscillator connection. An oscillator circuit is formed by connecting an external resistor and capacitor to these pins.	I	GND
OSCO	58		O	OPEN
$\overline{BLK}$	61	Display off control input. $\overline{BLK}$ = Low (V_{SS}) ... Display off. (S1 to S43 and G1 to G11 at V_{FL} level.) $\overline{BLK}$ = High (V_{DD}) ... Display on. Note that serial data can be transferred while the display is turned off.	I	GND
CL	63	Serial data transfer inputs. These pins must be connected to the system microcontroller. CL: Synchronization clock DI: Transfer data CE: Chip enable	I	GND
DI	64			
CE	62			
G1 to G11	2 to 12	Digit outputs. These pins are P-channel open drain outputs with pull-down resistors.	O	OPEN
S1 to S43	56 to 14	Segment outputs for displaying the display data transferred by serial data input. These pins are P-channel open drain outputs with pull-down resistors.	O	OPEN

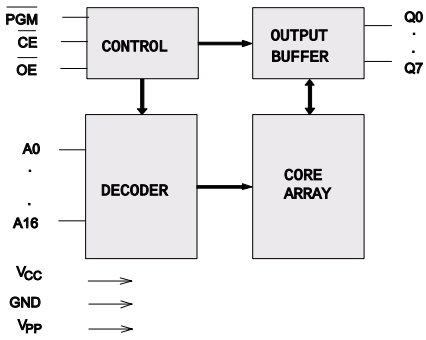
FEATURES

- High speed access time: 120/150 nS (max.)
- Read operating current: 10 mA (max.)
- Erase/Programming operating current: 30 mA (max.)
- Standby current: 20 µA (max.)
- Low voltage power supply range, 3.0V to 3.6V
- +14V erase/+12V programming voltage
- Fully static operation
- All inputs and outputs directly TTL/CMOS compatible
- Three-state outputs
- Available packages: 32-pin 600 mil DIP, 450 mil SOP and PLCC

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A16	Address Inputs
Q0–Q7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Enable
VPP	Program/Erase Supply Voltage
VCC	Power Supply
GND	Ground
NC	No Connection

1. ZIVA- 5 DVD CONTROLER

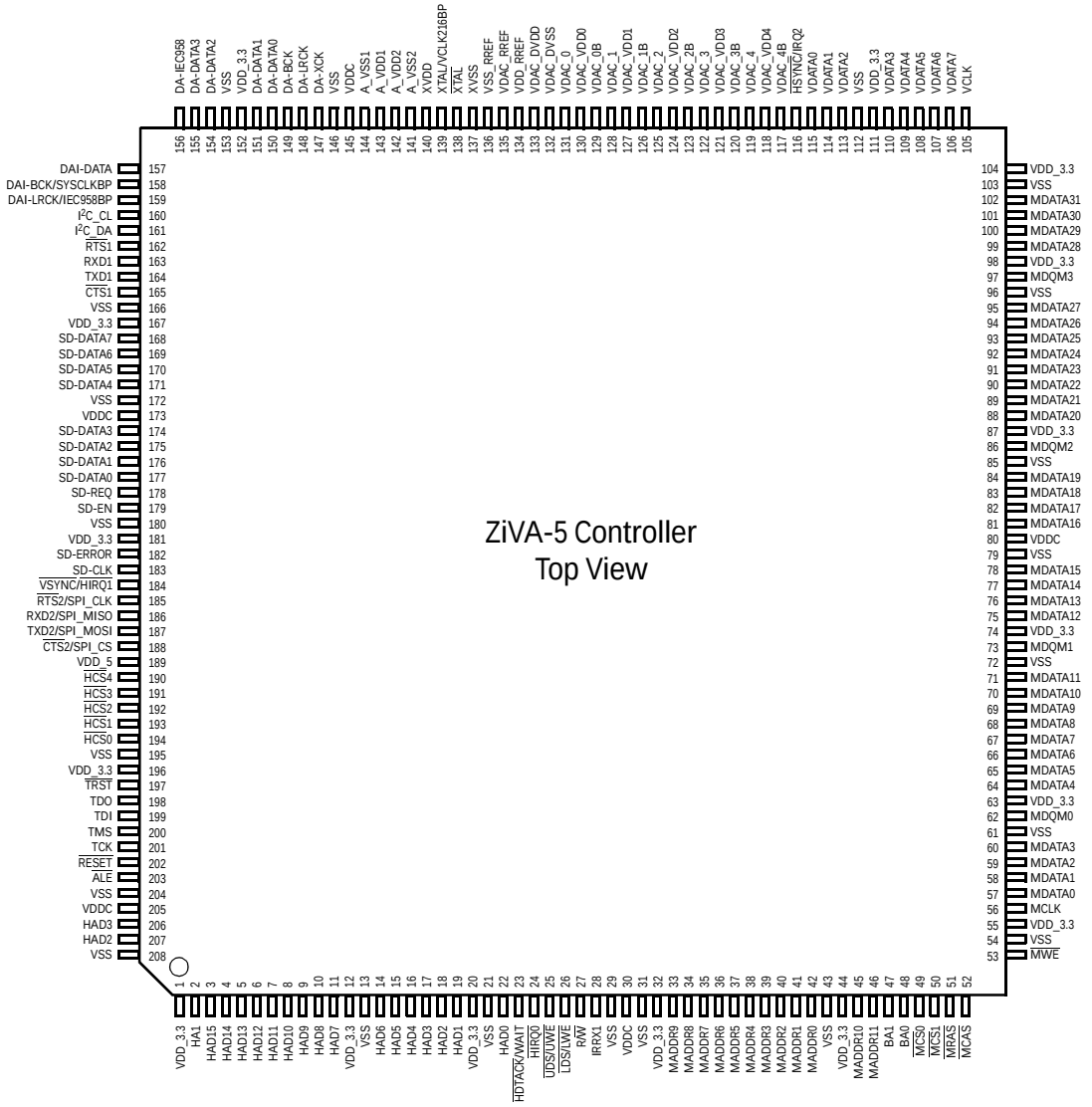


Figure 1 ZiVA-5 controller Pinout (208-pin PQFP)

Table 1 ZiVA-5 controller Pin List

Pin No.	Pin Name	I/O Voltage	I/O Type
1	VDDP	3.3V	ó
2	HA1	3.3V*	I/O
3	HA15	3.3V*	I/O
4	HA14	3.3V*	I/O
5	HA13	3.3V*	I/O
6	HA12	3.3V*	I/O

Table 1 ZiVA-5 controller Pin List (Continued)

Pin No.	Pin Name	I/O Voltage	I/O Type
7	HA11	3.3V*	I/O
8	HA10	3.3V*	I/O
9	HA9	3.3V*	I/O
10	HA8	3.3V*	I/O
11	HA7	3.3V*	I/O
12	VDDP	3.3V	ó
13	GNDP	GROUND	ó
14	HA6	3.3V*	I/O
15	HA5	3.3V*	I/O
16	HA4	3.3V*	I/O
17	HA3	3.3V*	I/O
18	HA2	3.3V*	I/O
19	HA1	3.3V*	I/O
20	VDDP	3.3V	ó
21	GNDP	GROUND	ó
22	HA0	3.3V*	I/O
23	$\overline{\text{HDTACK}}$/WAIT	3.3V*	I/OD
24	$\overline{\text{HIRQ0}}$	3.3V*	I/O
25	$\overline{\text{HUDS/UWE}}$	3.3V*	I/O
26	$\overline{\text{HLDS/LWE}}$	3.3V*	I/O
27	HREAD	3.3V*	I/O
28	IRRX1/GPIO[0]	3.3V*	I
29	GND	GROUND	ó
30	VDD	1.8V	ó
31	GND25	GROUND	ó
32	VDD25	3.3V	ó
33	MA9	3.3V	O
34	MA8	3.3V	O
35	MA7	3.3V	O
36	MA6	3.3V	O
37	MA5	3.3V	O
38	MA4	3.3V	O
39	MA3	3.3V	O
40	MA2	3.3V	O
41	MA1	3.3V	O
42	MA0	3.3V	O
43	GND25	GROUND	ó
44	VDD25	3.3V	ó
45	MA10	3.3V	O
46	MA11	3.3V	O
47	BA1	3.3V	O
48	BA0	3.3V	O
49	$\overline{\text{MCS0}}$	3.3V	O
50	$\overline{\text{MCS1}}$	3.3V	O
51	$\overline{\text{MRAS}}$	3.3V	O
52	$\overline{\text{MCAS}}$	3.3V	O
53	$\overline{\text{MWE}}$	3.3V	O

Table 1 ZiVA-5 controller Pin List (Continued)

Pin No.	Pin Name	I/O Voltage	I/O Type
54	GND25	GROUND	ó
55	VDD25	3.3V	ó
56	MCLK		O
57	MD0	3.3V	I/O
58	MD1	3.3V	I/O
59	MD2	3.3V	I/O
60	MD3	3.3V	I/O
61	GND25	GROUND	ó
62	MDQM0	3.3V	O
63	VDD25	3.3V	ó
64	MD4	3.3V	I/O
65	MD5	3.3V	I/O
66	MD6	3.3V	I/O
67	MD7	3.3V	I/O
68	MD8	3.3V	I/O
69	MD9	3.3V	I/O
70	MD10	3.3V	I/O
71	MD11	3.3V	I/O
72	GND25	GROUND	ó
73	MDQM1	3.3V	O
74	VDD25	3.3V	ó
75	MD12	3.3V	I/O
76	MD13	3.3V	I/O
77	MD14	3.3V	I/O
78	MD15	3.3V	I/O
79	GND	GROUND	ó
80	VDD	1.8V	ó
81	MD16	3.3V	I/O
82	MD17	3.3V	I/O
83	MD18	3.3V	I/O
84	MD19	3.3V	I/O
85	GND25	GROUND	ó
86	MDQM2	3.3V	O
87	VDD25	3.3V	ó
88	MD20	3.3V	I/O
89	MD21	3.3V	I/O
90	MD22	3.3V	I/O
91	MD23	3.3V	I/O
92	MD24	3.3V	I/O
93	MD25	3.3V	I/O
94	MD26	3.3V	I/O
95	MD27	3.3V	I/O
96	GND25	GROUND	ó
97	MDQM3	3.3V	O
98	VDD25	3.3V	ó
99	MD28	3.3V	I/O
100	MD29	3.3V	I/O

Table 1 ZiVA-5 controller Pin List (Continued)

Pin No.	Pin Name	I/O Voltage	I/O Type
101	MD30	3.3V	I/O
102	MD31	3.3V	I/O
103	GND25	GROUND	ó
104	VDD25	3.3V	ó
105	VCLK	3.3V*	I/O
106	VDATA7/GPIO[1]	3.3V*	I/O
107	VDATA6/GPIO[2]	3.3V*	I/O
108	VDATA5/GPIO[3]	3.3V*	I/O
109	VDATA4/GPIO[4]	3.3V*	I/O
110	VDATA3/GPIO[5]	3.3V*	I/O
111	VDDP	3.3V	ó
112	GNDP	GROUND	ó
113	VDATA2/GPIO[6]	3.3V*	I/O
114	VDATA1/GPIO[7]	3.3V*	I/O
115	VDATA0/GPIO[8]	3.3V*	I/O
116	$\overline{\text{HSYNC}}$/$\overline{\text{HIRQ2}}$/GPIO[9]	3.3V*	I/O
117	VDAC_4B	ANALOG	O
118	VDAC_VDD4	3.3V ANALOG	ó
119	VDAC_4	ANALOG	O
120	VDAC_3B	ANALOG	O
121	VDAC_VDD3	3.3V ANALOG	ó
122	VDAC_3	ANALOG	O
123	VDAC_2B	ANALOG	O
124	VDAC_VDD2	3.3V ANALOG	ó
125	VDAC_2	ANALOG	O
126	VDAC_1B	ANALOG	O
127	VDAC_VDD1	3.3V ANALOG	ó
128	VDAC_1	ANALOG	O
129	VDAC_0B	ANALOG	O
130	VDAC_VDD0	3.3V ANALOG	ó
131	VDAC_0	ANALOG	O
132	VDAC_DVSS	GROUND	
133	VDAC_DVDD 3.	3V	
134	VAC_REFVDD	3.3V	
135	VDAC_REF	ANALOG	I
136	VDAC_REFVSS	GROUND	
137	XVSS	GROUND	
138	XOUT	ANALOG	
139	XIN/bypass clk_216	ANALOG	
140	XVDD	3.3V	
141	AVSS2	GROUND	
142	AVDD2	3.3V	
143	AVDD1	3.3V	
144	AVSS1	GROUND	
145	VDD	1.8V	ó
146	GND	GROUND	ó
147	XCK	3.3V*	I/O

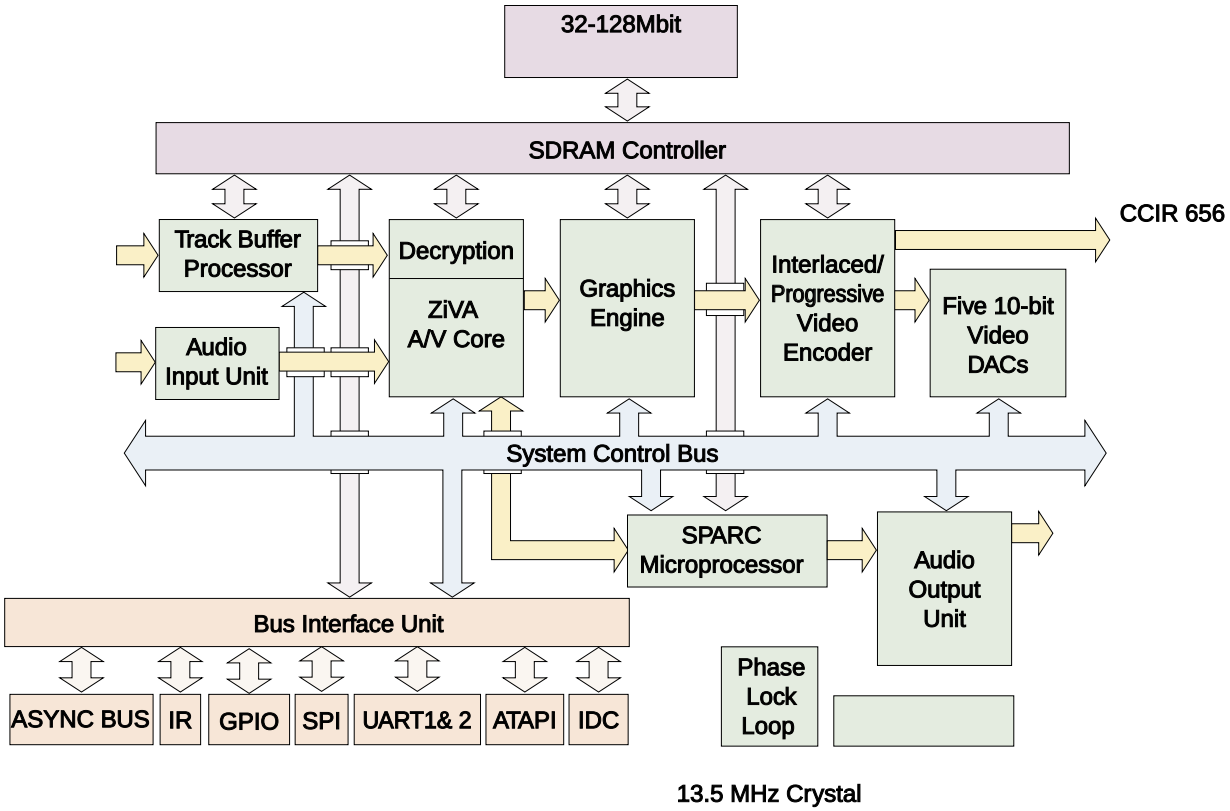
Table 1 ZiVA-5 controller Pin List (Continued)

Pin No.	Pin Name	I/O Voltage	I/O Type
148	LRCK	3.3V*	O
149	BCK	3.3V*	O
150	ADATA0/GPIO[10]	3.3V*	O
151	ADATA1/GPIO[11]	3.3V*	O
152	VDDP	3.3V	ó
153	GNDP	GROUND	ó
154	ADATA2/GPIO[12]	3.3V*	O
155	ADATA3/GPIO[13]	3.3V*	O
156	IEC958/GPIO[14]	3.3V*	O
157	DAI_DATA/GPIO[15]	3.3V*	I
158	DAI_BCK/bypass_sysclk/ GPIO[16]	3.3V*	I
159	DAI_LRCK/iec958bp/GPIO[17]	3.3V*	I
160	I2C_CL/GPIO[18]	3.3V*	I/OD
161	I2C_DA/GPIO[19]	3.3V*	I/OD
162	$\overline{\text{RTS}}$1/GPIO[20]	3.3V*	O
163	RXD1/GPIO[21]	3.3V*	I
164	TXD1/GPIO[22]	3.3V*	O
165	$\overline{\text{CTS}}$1/GPIO[23]	3.3V*	I
166	GNDP	GROUND	ó
167	VDDP	3.3V	ó
168	SDDATA7/VDATA2[7]/ HDMARQ/GPIO[24]	3.3V	I
169	SDDATA6/VDATA2[6]/HXCVR_ EN/ GPIO[25]	3.3V*	I
170	SDDATA5/VDATA2[5]/ HDMACK/GPIO[26]	3.3V*	I
171	SDDATA4/VDATA2[4]/GPIO[27]	3.3V*	I
172	GND	GROUND	ó
173	VDD	1.8V	ó
174	SDDATA3/VDATA2[3]/GPIO[28]	3.3V*	I
175	SDDATA2/VDATA2[2]/GPIO[29]	3.3V*	I
176	SDDATA1/VDATA2[1]/GPIO[30]	3.3V*	I
177	SDDATA0/VDATA2[0] /GPIO[31]	3.3V*	I
178	SDREQ/GPIO[32]	3.3V*	O
179	SDEN/GPIO[33]	3.3V*	I
180	GNDP	GROUND	ó
181	VDDP	3.3V	ó
182	SDERROR/GPIO[34]	3.3V*	I
183	SDCLK/GPIO[35]	3.3V*	I
184	$\overline{\text{VSYNC}}$/$\overline{\text{HIRQ1}}$/GPIO[36]	3.3V*	I/O
185	$\overline{\text{RTS}}$2/SPI_CLK/GPIO[37]	3.3V*	O
186	RXD2/SPI_MISO/GPIO[38]	3.3V*	I
187	TXD2/SPI_MOSI/GPIO[39]	3.3V*	O
188	$\overline{\text{CTS}}$2/SPI_CS/GPIO[40]	3.3V*	I
189	VNW	5V	ó

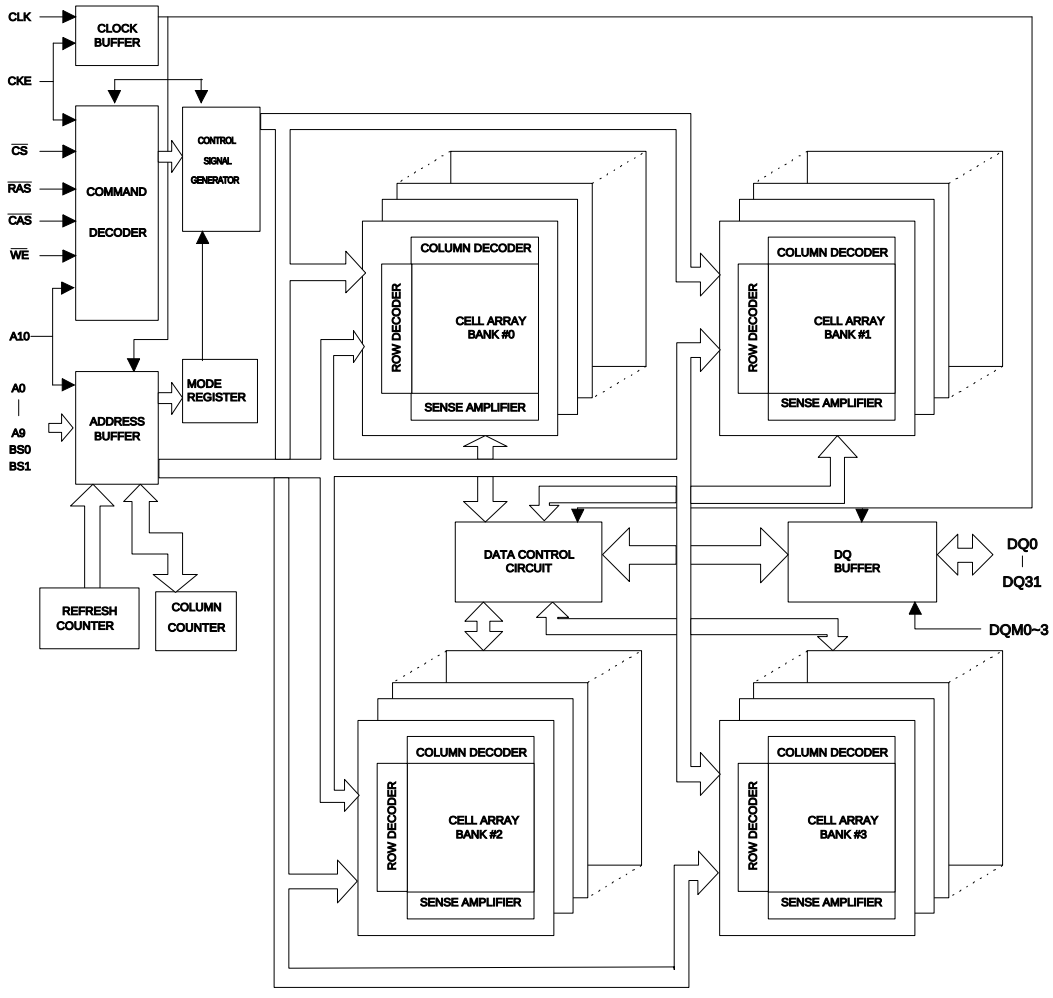
Table 1 ZiVA-5 controller Pin List (Continued)

Pin No.	Pin Name	I/O Voltage	I/O Type
190	$\overline{HCS4}$/GPIO[41]	3.3V*	I
191	$\overline{HCS3}$/GPIO[42]	3.3V*	I
192	$\overline{HCS2}$/GPIO[43]	3.3V*	I
193	$\overline{HCS1}$	3.3V*	I/O
194	$\overline{HCS0}$	3.3V*	I/O
195	GNDP	GROUND	ó
196	VDDP	3.3V	ó
197	$\overline{TRST}$	3.3V*	I
198	TDO	3.3V*	O
199	TDI/GPI[0]	3.3V*	I
200	TMS/GPI[1]	3.3V*	I
201	TCK	3.3V*	I
202	$\overline{RESET}$	3.3V*	I
203	$\overline{ALE}$	3.3V*	I/O
204	GND	GROUND	ó
205	VDD	1.8V	ó
206	HA3	3.3V*	I
207	HA2	3.3V*	I
208	GNDP	GROUND	ó

Note: The ZiVA-5 core operates at 1.8V ± 10%. Most I/O interface pins can be interfaced with 3.3-V or 5-V devices depending on the voltage applied to the VDD pins associated with them. Refer to the Application Note for more information.

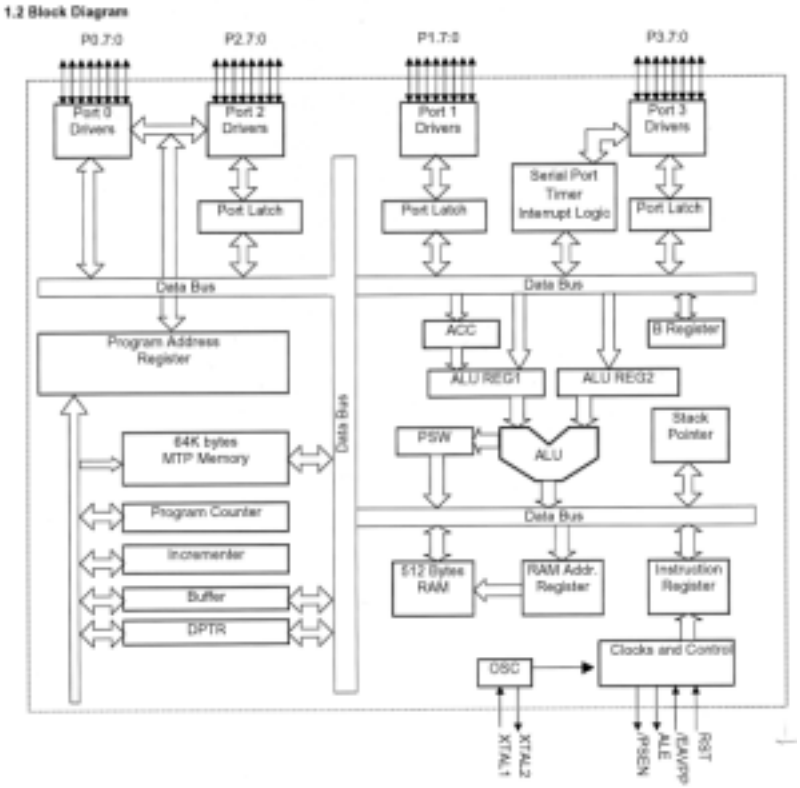


BLOCK DIAGRAM

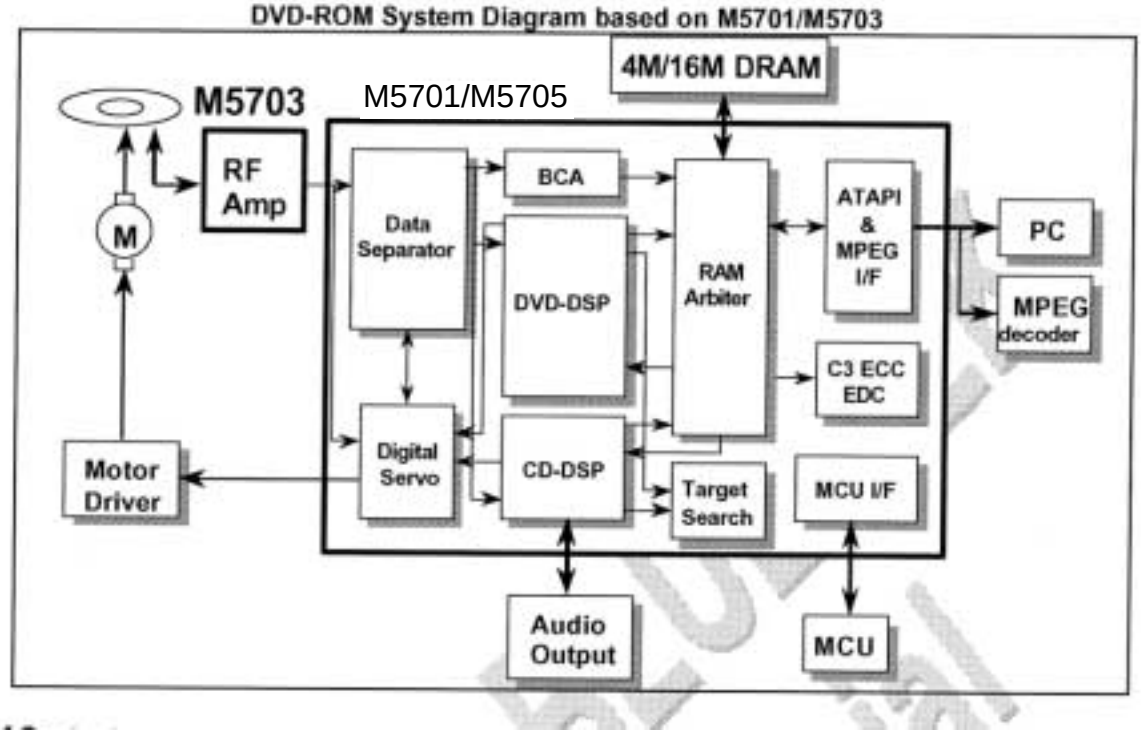


NOTE:
The cell array configuration is 2048 * 256 * 32

3. M6759 ; 8BIT MTP micro controller

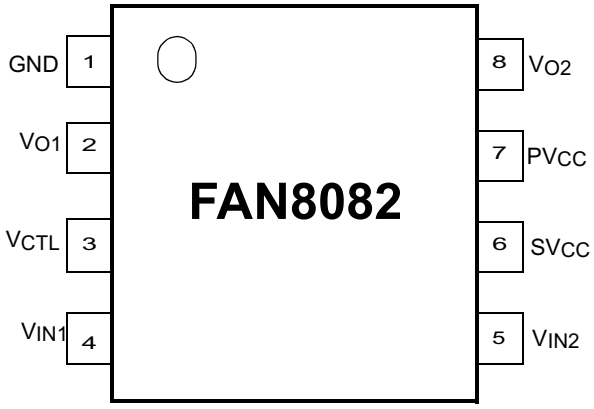


4. M5701/M5705 ; DVD ROM controller



5. FAN8082

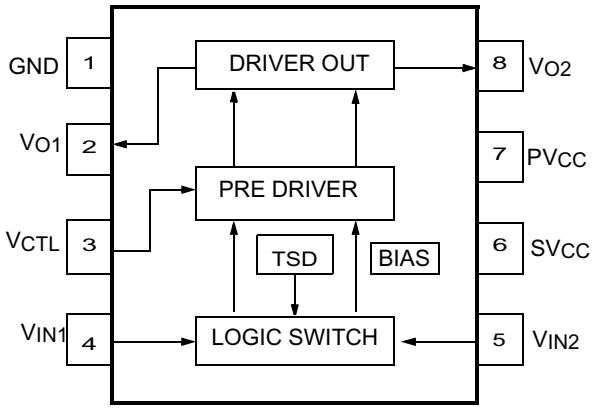
Pin Assignments



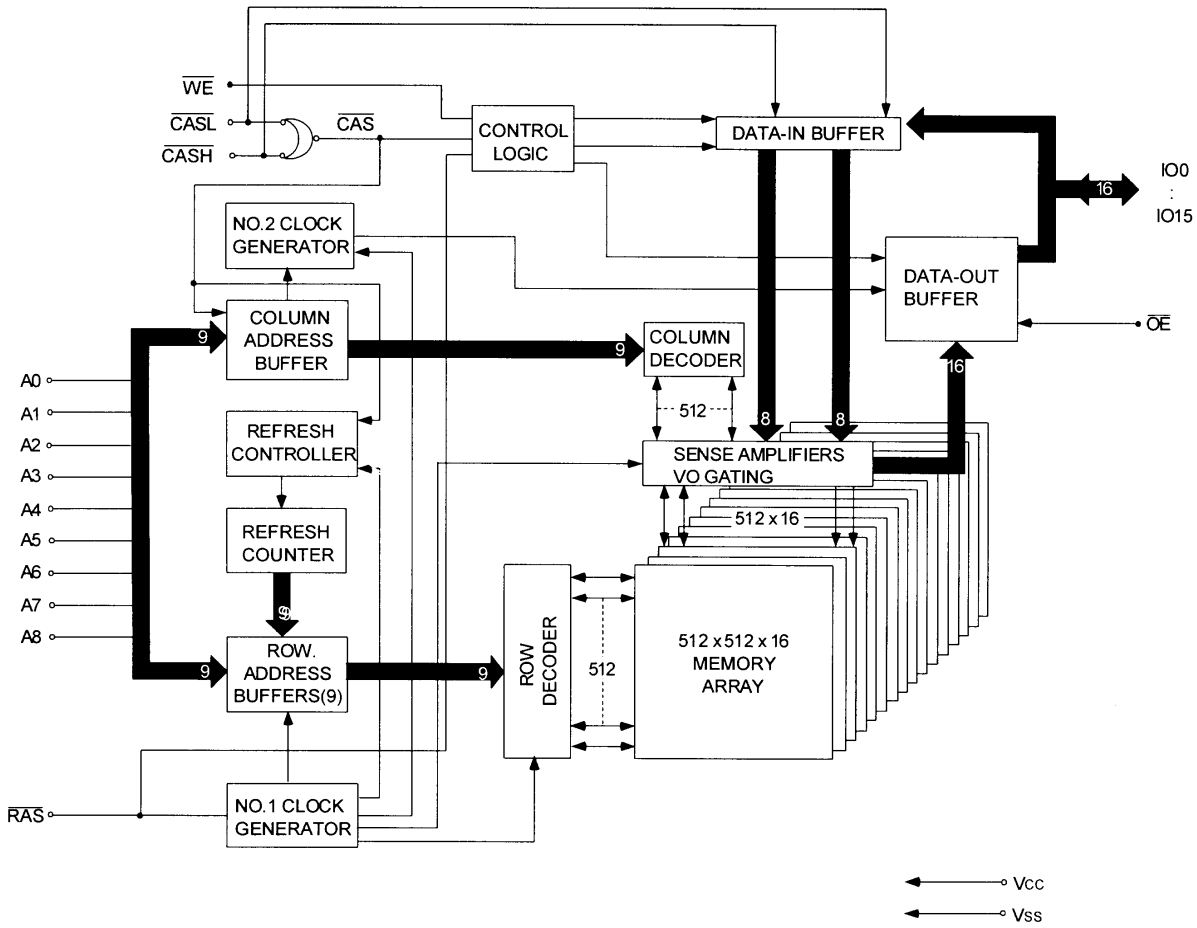
Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	GND	-	Ground
2	V_{O1}	O	Output 1
3	V_{CTL}	I	Motor speed control
4	V_{IN1}	I	Input 1
5	V_{IN2}	I	Input 2
6	SV_{CC}	-	Supply voltage (Signal)
7	PV_{CC}	-	Supply voltage (Power)
8	V_{O2}	O	Output 2

Internal Block Diagram

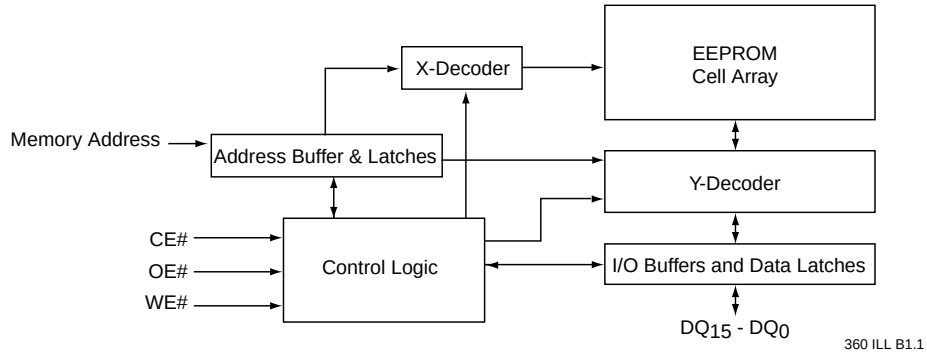
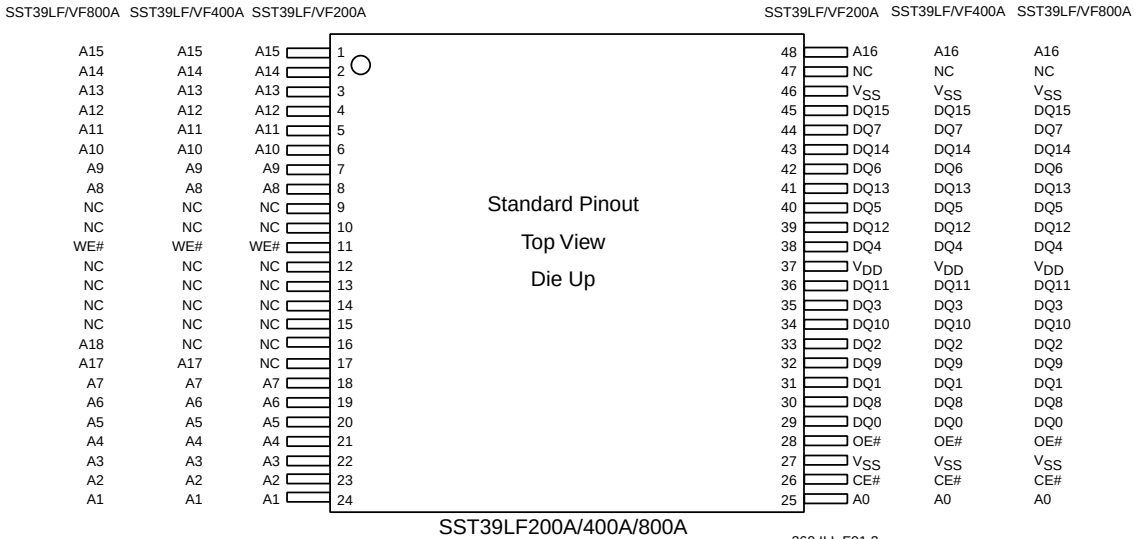


FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NO.	SYM.	TYPE	DESCRIPTION
16~19,22~26	A0~A8	Input	Address Input
14	$\overline{RAS}$	Input	Row Address Strobe
28	$\overline{CASH}$	Input	Column Address Strobe/Upper Byte Control
29	$\overline{CASL}$	Input	Column Address Strobe/Lower Byte Control
13	$\overline{WE}$	Input	Write Enable
27	$\overline{OE}$	Input	Output Enable
2~5,7~10,31~34,36~39	I/O0 ~ I/O15	Input/Output	Data Input/Output
1,6,20	Vcc	Supply	Power, 5V
21,35,40	Vss	Ground	Ground
11,12,15,30	NC	-	No Connect

7. SST39LF800A ; Multi Purpose Flash

FUNCTIONAL BLOCK DIAGRAM